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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/599,832	10/11/2006	Takaharu Tanaka	P30819	5260

52123 7590 03/01/2010

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EXAMINER	
HOANG, PHI	
ART UNIT	PAPER NUMBER
2628	

NOTIFICATION DATE	DELIVERY MODE
03/01/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/599,832	TANAKA ET AL.	
	Examiner	Art Unit	
	PHI HOANG	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 8-17, filed 19 November 2009, with respect to the rejection(s) of claim(s) 13-26 under 35 U.S.C. 112 and 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Srinivasan et al.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 13, 14 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US 6,075,899) in view of Srinivasan et al. (US 2003/0113026 A1).

4. Regarding claim 13, Yoshioka discloses an information processing device comprising: a DRAM having a burst mode which burst-transfers data of successive column addresses; (Column 8, lines 5-27)

at least one processing unit operable to issue an access request; (Column 14, lines 20-27)

and an address conversion unit operable to convert access addresses which are included in the access request issued from said at least one processing unit, (Column 3, lines 29-35)

wherein at least one of said at least one data processing unit is operable to access an M x N rectangular area, where M and N are integers, (Column 7, lines 38-43)

said address conversion unit is operable to convert access addresses so that a column address of data at a (K+m)th column, where K and m are integers and $m \leq M$, of an Lth line, and a column address of data at a Kth column of an (L+n)th line, where L and n are integers and $n \leq N$ become successive, (Column 3, lines 29-35, burst length defines how many columns are read)

and at least one area of said DRAM is a frame memory which stores image data, the rectangular area is M pixels x N lines in the image data, and said at least one data processing unit is operable to perform one of motion compensation and motion estimation, where n=2n' and n' is an integer (Column 7, lines 16-21).

Yoshioka does not clearly disclose L, n, and n' are positive integers resulting in a positive (L+n)th line not being read.

Srinivasan discloses not encoding of a row of macroblocks of pixels based on a flag that determines whether the row should be skipped or not and if it is skipped the next row of macroblocks are checked again for the same flag (Paragraphs 0131-0132).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yoshioka to avoid reading in certain rows of

pixels for processing as disclosed by Srinivasan because unnecessary processing and loss in time is prevented.

5. Regarding claim 14, Yoshioka (Column 14, lines 17-27, processor reads from a first in, first out memory) in view of Srinivasan discloses another data processing unit is operable to access the image data on a line basis, and to continuously read out data of all 2n lines.

6. Regarding claim 23, Yoshioka discloses a data access method for accessing a rectangular area made up of M pixels x N lines in image data from a DRAM, Column 7, lines 38-43) the DRAM having a burst mode which burst-transfers data of continuous column addresses, and storing the image data (Column 8, lines 5-27), said the access method comprising:

inputting an access request for the rectangular area; (Column 14, lines 17-43)

and converting access addresses included in the access request (Column 3, lines 29-35),

the addresses are converted so that a column address of data at a (K+m)th column, where K and m are integers and $m \leq M$, of the Lth line, and a column address of the data at the Kth column of the (L+n) line, where L and n are integers and $n \leq N$, become successive, (Column 3, lines 29-35, burst length defines how many columns are read)

and at least one area of said DRAM is a frame memory which stores image data and the rectangular area is M pixels x N lines in the image data, where M and N are

integers, and a data processing unit performs motion compensation and motion estimation, where n=2n' and n' is an integer (Column 7, lines 16-21).

Yoshioka does not clearly disclose L, n, and n' are positive integers resulting in a positive (L+n)th line not being read.

Srinivasan discloses not encoding of a row of macroblocks of pixels based on a flag that determines whether the row should be skipped or not and if it is skipped the next row of macroblocks are checked again for the same flag (Paragraphs 0131-0132).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yoshioka to avoid reading in certain rows of pixels for processing as disclosed by Srinivasan because unnecessary processing and loss in time is prevented.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US 6,075,899) in view of Srinivasan et al. (US 2003/0113026 A1) and further in view of Mitsuishi (US 6,745,320 B1).

8. Regarding claim 15, Yoshioka in view of Srinivasan discloses said at least one data processing unit is operable to decode an inputted stream on a basis of at least two macroblocks, by motion compensation, (Column 1, line 50 – column 2, line 4)

said DRAM is operable to store the image data decoded by said data processing unit, (Column 2, lines 12-20)

and said at least one data processing unit is operable to access the image data stored in said DRAM as reference data. (Column 2, line 21 column 2, line 36)

Yoshioka in view of Srinivasan does not clearly disclose said information processing device further comprises: a memory featuring a smaller storage capacity and a faster access speed than said DRAM; a data transfer unit operable to transfer the data from said DRAM to said memory.

However, it is well known in the art that processors have small, fast memory called registers built in for quick access to data from memory (RAM) for processing. Mitsuishi discloses a general purpose processor with registers available for high speed processing (Column 12, lines 6-18).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yoshioka in view of Srinivasan to utilize smaller, faster memory for processing as disclosed by Mitsuishi because processing of data can be performed more quickly.

9. Claims 16-22 and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (US 6,075,899) in view of Srinivasan et al. (US 2003/0113026 A1) in view of Mitsuishi (US 6,745,320 B1) and further in view of Callway et al. (US 6,807,311 B1).

10. Regarding claim 16, Yoshioka in view of Srinivasan and further in view of Mitsuishi discloses all limitations discussed in claim 15.

Yoshioka (Column 14, lines 17-27, accessing data from memory) in view of Srinivasan and further in view of Mitsuishi (Column 12, lines 6-18, transferring data to other faster memory) further disclose said data transfer unit is operable to transfer data

on a transfer region basis from said DRAM to said memory, based on the access request from said data processing unit.

Yoshioka in view of Srinivasan and further in view of Mitsuishi does not disclose the image data stored in said DRAM is split into transfer regions larger in size than the rectangular area.

Callway discloses the image data stored in said DRAM is split into transfer regions larger in size than the rectangular area (Column 12, lines 42-58).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yoshioka in view of Srinivasan and further in view of Mitsuishi to segment regions of an image for transfer because bandwidth usage is reduced by only retrieving the regions that are necessary.

11. Regarding claim 17, Yoshioka in view of Srinivasan and further in view of Mitsuishi discloses all limitations discussed in claim 15.

Yoshioka in view of Srinivasan and further in view of Mitsuishi does not disclose said data transfer unit is operable to transfer a minimum area which surrounds plural rectangular areas as a transfer region as data from said DRAM to said memory, based on an access request from said at least one data processing unit.

Callway discloses said data transfer unit is operable to transfer a minimum area which surrounds plural rectangular areas as a transfer region as data from said DRAM to said memory, based on an access request from said at least one data processing unit (Column 12, lines 42-58, area is fixed).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yoshioka in view of Srinivasan and further in view of Mitsuishi to transfer a fixed area because bandwidth usage can be reduced by using an optimal size for each transfer.

12. Regarding claim 18, Yoshioka in view of Srinivasan in view of Mitsuishi and further in view of Callway (Column 12, lines 42-58, since the area for transfer is a fixed size the value of the fixed sized is inherently stored in a memory) discloses said data transfer unit includes a register which holds a size of the transfer region.

13. Regarding claim 19, Yoshioka (Column 14, lines 17-27, the processor accesses the image in memory once) in view of Srinivasan in view of Mitsuishi (Column 12, lines 6-18, discloses transferring from RAM to registers) and further in view of Callway discloses said data transfer unit is operable to transfer the data from said DRAM to said memory when a predetermined number n1 of access requests are outputted from said at least one data processing unit.

14. Regarding claim 20, Yoshioka (Column 14, lines 17-27, the processor accesses the image in memory once) in view of Srinivasan in view of Mitsuishi and further in view of Callway (Column 12, lines 42-58, since the area for transfer is a fixed size the value of the fixed sized is inherently stored in a memory) discloses said data transfer unit includes a register which holds the size of the transfer region and the predetermined number n1.

15. Regarding claim 21, Yoshioka in view of Srinivasan in view of Mitsuishi and further in view of Callway (Column 12, lines 42-58, since the transfer unit is transferring all rectangular areas, there is no regard to whether it is adjacent or overlapping) discloses said data transfer unit is operable to transfer the transfer region which includes all rectangular areas, from said DRAM to said memory when access requests from said at least one data processing unit request the rectangular areas which are adjacent or overlapping.

16. Regarding claim 22, Yoshioka (Column 3, lines 53-67 and column 9, line 13 – column 14, line 7, half-pel interpolation is performed (motion vector estimation) on an image and then decoded) in view of Srinivasan in view of Mitsuishi and further in view of Callway discloses a motion vector estimation unit operable to estimate plural motion vectors corresponding to plural macroblocks from the inputted stream; and a decoding unit operable to decode the inputted stream on a macroblock basis, and to store a decoding result into said DRAM, wherein a decoding sequence of the macroblocks is changed based on the plural motion vectors so that addresses for accessing said DRAM become successive.

17. Regarding claim 24, Yoshioka (Column 14, lines 17-27, the processor accesses the image in memory once) in view of Srinivasan in view of Mitsuishi (Column 12, lines 6-18, discloses transferring from RAM to registers) and further in view of Callway discloses said data transfer unit is operable to transfer the data from said DRAM to said

memory when a predetermined number n1 of access requests are outputted from said data processing unit.

18. Regarding claim 25, Yoshioka (Column 14, lines 17-27, the processor accesses the image in memory once) in view of Srinivasan in view of Mitsuishi and further in view of Callway (Column 12, lines 42-58, since the area for transfer is a fixed size the value of the fixed sized is inherently stored in a memory) discloses said data transfer unit includes a register which holds a size of the transfer region and the predetermined number n1.

19. Regarding claim 26, Yoshioka in view of Mitsuishi and further in view of Callway (Column 12, lines 42-58, since the transfer unit is transferring all rectangular areas, there is no regard to whether it is adjacent or overlapping) in view of Srinivasan discloses said data transfer unit is operable to transfer the transfer region which includes all rectangular areas, from said DRAM to said memory when access requests from said at least one data processing unit request the rectangular areas which are adjacent or overlapping.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHI HOANG whose telephone number is 571-270-3417. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on 571-272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Phi Hoang/
Examiner, Art Unit 2628
February 24, 2010

/XIAO M. WU/
Supervisory Patent Examiner, Art Unit 2628